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09/943,149	08/30/2001	Nathan Y. Moyal	0325.00495	8648

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EXAMINER

NGUYEN, LINH V

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/943,149

Applicant(s)

MOYAL ET AL.

Examiner

Linh V. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

***R sponse to Amendment***

1. This office action is in response to Amendment received on 07/25/03. Claims 1, 15 and 16 have been amended. Claims 1 – 21 are pending on this application.

***Response to Arguments***

2. Applicant's arguments with respect to claims 14, and 21 have been considered but not persuasive from the following:

Regarding to new claim 21, Fig. 1 of Gotz et al. disclose a lock circuit (CL) configured to generate a lock signal (output of CL connected to MUX1 and MUX2) in response to an external input (out put of US is an external input to CL).

Regarding to claim 14, where in second and third dividers comprise multi-channel dividers (page 2 lines 4 –6, disclosing PLL circuit for TDMA, GSM systems, because Time Division Multiple Access (TDMA) or Global system for Mobile Communication (GSM) is a multi-channel communication system.

3. Applicant's arguments with respect to amended claims 1, 15 and 16 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claim 21 is rejected under 35 U.S.C. 102(a) as being anticipated by Gotz et al. German patent No. 19946200 A1 (English translation US2002/0153959 A1).

Fig. 1, of Gotz et al. disclose an apparatus comprising: a phase lock loop (Fig. 1), configured to multiply an input frequency (FT4) to generate an output frequency in response to a lock signal (output from control logic (CL)); and a lock circuit (CL) configured to generate said lock signal in response to an external input (out put signal of US is an external input signal to CL, wherein said PLL is configured (MUX) to (i) select a reference frequency as said input frequency when in a first mode (output of FT3) and (ii) select a divided frequency (output of FT4) of said input frequency as said input frequency with in a second mode , wherein either said first mode or said second mode is selected in response to said lock signal (output of CL).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 – 4, 6, and 9 – 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gotz et al. as applied to claim 21 above.

Regarding to claims 1, Fig. 1 of Gotz et al. disclose a phase lock loop having MUX1 and MUX2 response to a lock signal output from control logic (CL) to select a

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reference frequency (MUX2) as said input frequency (output from FT3) and select a first feedback ratio (MUX1) when in a first mode; and select a divided frequency (output from FT4) of said input frequency as said input frequency and select a second feedback ratio (MUX1), when in a second mode; wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio ( this is inherently to Gotz et al., because the first bit and the second bit are intrinsic for selection of MUX1 or MUX2) Although Gotz et al. is silence to the term "multi-bit" lock signal from his lock signal for MUX1 and MUX2, but the lock signal of Gotz et al is providing the same function and concept of the multi-bit lock signal of claimed invention, therefore the term "multi-bit" must be intrinsic or inherently to the lock signal of Gotz et al. Furthermore applicant fails to point out the "multi-bit" of claimed invention is having any elements or structures which are distinct over the lock signal of Gotz et al, besides the terminology of "multi-bit".

Above discussed, Gotz et al. disclose every aspect of applicant's claimed invention except for wherein said divided frequency is adjustable in response to said multi-bit lock signal.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the divided frequency of Gotz et al. adjustable, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art . In re Stevens, 101 USPQ 284 (CCPA 1954).

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Regarding to claim 2, Gotz et al. as applied to claim 1 above, further disclose wherein the first mode is further configured to increase a feedback divide ratio (f2MUX1).

Regarding to claim 3, Gotz et al. as applied to claim 1 above, further disclose wherein the second mode is further configured to decrease the feedback divide ratio (f1MUX1).

Regarding to claim 4, Gotz et al. as applied to claim 1 above, further disclose wherein the lock circuit comprises a lock decision logic circuit (CL).

Regarding to claim 6, Gotz et al. as applied to claim 1 above, further disclose wherein the lock circuit is configured in response to an internal/external signal (output signal of change over control circuit (US)).

Regarding to claim 9, Gotz et al. as applied to claim 1 above, further disclose wherein the PLL comprises: a first switchable divider (MUX2) configured to generate a reference frequency in response to the input frequency; a PLL logic circuit configured to generate the output frequency (fVCO) in response to the reference; and a second switchable divider (MUX1) configured to generate feedback frequency in response to said output frequency.

Regarding to claim 10, Gotz et al. as applied to claim 1 above, further disclose wherein said first and second switchable dividers are further configured in response to said lock signal (see Fig. 1).

Regarding to claim 11, Gotz et al. as applied to claim 1 above, further disclose wherein the first switchable divider comprises a first divider (FT4) and a first multiplexer

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(MUX2), wherein the first multiplexer is configured to select the first divided output frequency or the input frequency and present the reference frequency; and the second switchable divider comprises a second divider (FT1), a third divider (FT2) and a second multiplexer (MUX1), wherein said multiplexer is configured to select a second divided output frequency or a third divided frequency and present the feedback frequency (f1MUX1, f2MUX1).

Regarding to claim 12, Gotz et al. as applied to claim 1 above, further disclose wherein said second and third dividers are configured in series (FT1, FT2).

Regarding to claim 14, Gotz et al. as applied to claim 1 above, further disclose where in second and third dividers comprise multi-channel dividers (page 2 lines 4 –6, disclosing PLL circuit for TDMA, GSM systems, because TDMA or GSM is a multi-channel communication system).

Regarding to Claim 13, Gotz et al. as applied to claim 11 above disclose every aspect of applicant's claimed invention except that wherein said second and third dividers are configured in parallel. Fig. 1 Gotz et al. shows dividers (FT, FT2) circuit arrangement is an equivalent structure known in the art and furthermore this equivalent circuit also has indicated by applicant with respect to Fig. 5, 6 or Fig. 7, 8 of applicant application. Therefore Gotz et al. structures are equivalent to applicant's claimed invention.

Regarding to claims 15 – 20, the steps in the claimed method are deemed to be made clearly taught by Gotz et al. as applied to claims 1 – 4, 9 – 12, and 14 above.

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8. Claims 5, 7 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Gotz et al. in view of Lada, Jr. et al. U.S patent No. 5, 142, 247.

Gotz et al. as applied to claim 1 above disclose every aspect of applicant's claimed invention except wherein the control logic circuit comprises a timer, and a user externally controls the lock circuit.

Fig. 2 Lada discloses a Phase Lock Loop circuit having a lock logic circuit (30) externally controlled by a user (SEL) to generate a lock signal (REFSEL) wherein the lock logic circuit is external comprises a timer (33).

Gotz et al. and Lada, Jr. et al., are analogous because they are from similar problem solving for Phase Lock Loop circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply external control of lock logic circuit with timer of Lada et al. to the internal control of lock logic circuit of Gotz et al. for the purpose of maintaining the pulse for a predetermined number of cycles so that the pulse duration exceeds the time necessary for Phase Lock Loop to acquire and lock onto the new frequency (Lada, Col. 6 lines 41 – 47).

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone



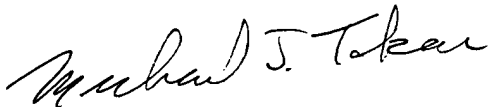
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numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

August 26, 2003

  
Michael Tokar  
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